DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 24 February 2010 has been entered.

Response to Amendment

Applicant's amendment filed 24 February 2010 has been entered. Claims 1, 4 and 7 have been amended. Claims 1-7, 10, 11 and 14-16 are still pending in this application with claim 1, 4, and 7 being independent. Please note that AU 2416 has been changed to AU 2474.

EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Kavon Nasabsedeh (Reg. No. 62,721) on 24 February 2010.

The application has been amended as follows:

Please replace claims 3, 6, 11 and 14 with the following:

3. The method according to claim 2, further comprising:

configuring, in accordance with the first bit rate, a first bit allocation table for the symbols transmitted during the first noise phase; and

configuring, in accordance with the second bit rate, a second bit allocation table for the symbols transmitted during the second noise phase.

6. The apparatus according to claim 5, wherein the constrained rate receiver further comprises:

a first bit allocation table controller for configuring, in accordance with the first bit rate, a first bit allocation table for the symbols transmitted during the first noise phase; and

a second bit allocation table controller for configuring, in accordance with the second bit rate, a second bit allocation table for the symbols transmitted during the second noise phase.

11. The constrained rate receiver according to claim 10, further comprising:

a first bit allocation table controller for configuring, in accordance with the first bit rate, a first bit allocation table for the symbols transmitted during the first noise phase; and

a second bit allocation table controller for configuring, in accordance with the second bit rate, a second bit allocation table for the symbols transmitted during the second noise phase.

14. The constrained rate receiver according to claim 7, wherein the first bit rate controller comprises a controller for determining the first bit rate in accordance with the following equation:

$$R_1 = -R_2 * \frac{S_2}{S_1} * \frac{latency * C + SymTime * S_1}{latency * C - SymTime * S_2}$$

wherein R_1 is the first bit rate, R_2 is the second bit rate, latency is the predetermined maximum allowed transmission latency, and SymTime is [[a]] the discrete multi-tone symbol duration, for S_2 symbols of the second nose phase transmitted during [[a]] the number C of noise clock cycles and S_1 symbols of the first noise phase transmitted during the number C of noise clock cycles.

3. The following is an examiner's statement of reasons for allowance:

Claims 1-7, 10-11 and 14-16 are allowable over the prior art since none of the prior art taken either alone or in combination particularly discloses, fairly suggests, or renders obvious each and every claimed limitation. In particular, the novel feature of the claims is that the first bit rate is determined by an algebraic equation of a combination of definite values while ensuring that the transmission latency does not exceed a pre-determined maximum allowed transmission latency.

Prior art reference to Matsumoto (US 6.747,992) discloses a communication system that aims to minimize the delay time by decreasing the difference between the bitmaps A and B.

However, Matsumoto does not teach determining the first bit rate from an algebraic equation including the second bit rate, the pre-determined maximum allowed transmission latency, a discrete multi-tone symbol duration, and a number of symbols of the first and second noise phase transmitted during a number of noise clock cycles.

Prior art reference to Okamura (US 6,658,024) aims to minimize the delay in both normal and noisy conditions. However, Okamura merely minimizes the delay on certain data types (fast data) regardless of noise levels. Okamura does not teach that the delay is made not to exceed a predetermined maximum allowed transmission latency while determining a first bit rate by an algebraic equation including the second bit rate, the pre-determined maximum allowed transmission latency, a discrete multi-tone symbol duration, and numbers of symbols of the first and second noise phases transmitted during a number of noise clock cycles.

Therefore, neither the above-mentioned prior art references, nor the other prior art of record, teach, either alone or in combination, each and every limitation of the independent claims, including increasing the difference between the bit rate during the first noise phase and the bit rate during the second noise phase while also ensuring that the transmission latency does not exceed a pre-determined maximum allowed transmission latency.

Regarding the issue of Subject Matter Eligibility, the claims satisfy the requirements of 35 USC 101. Method claim 1 satisfies the requirements of 35 USC 101 because the method uses a particular machine (transmitter to transmit symbols) and does not pre-empt substantially all

practical uses of a judicial exception (the algebraic equation is limited to the scope of determining the bit rate according to a transmission system that controls transmission latency). Apparatus claim 4 satisfies the requirements of 35 USC 101 because the apparatus, while using an equation to perform its functions, is directed to a practical application of the equation, but does not cover all practical applications (again the equation is limited to the scope of determining the bit rate according to a transmission system that controls transmission latency). Similarly, the constrained rate receiver claim 7 also satisfies the requirements of 35 USC 101 because the receiver uses the algebraic equation to arrive at a bit rate that allows the latency to not exceed a predetermined maximum allowed transmission latency for controlling the communication system (this practical application of the equation does not cover substantially all practical applications of the judicial exception).

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Curtis A. Alia whose telephone number is (571) 270-3116. The examiner can normally be reached on Monday through Friday, 9am-6pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Aung S. Moe can be reached on (571) 272-7314. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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Supervisory Patent Examiner, Art Unit 2474

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Examiner, Art Unit 2474
3/26/2010

CAA